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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,017	11/27/2001	Rene Toutant	86177-23	1111

7590 05/08/2006

SMART & BIGAR
Suite 3400
1000 de la Gauchetiere Street West
Montreal, QC H3B 4W5
CANADA

EXAMINER	
SOL, ANTHONY M	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,017	TOUTANT ET AL.	
	Examiner	Art Unit	
	Anthony Sol	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed 1/26/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

- Applicant's Amendment filed 1/26/2006 is acknowledged.
- The amendments to Figs, 4A, 5A, and 6 filed 1/26/2006 are approved.
- Claims 1, 21, 31, and 35 have been amended.
- No claims have been added.
- No claims have been canceled.
- Claims 1-35 remain pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-8,10-13, 15-17 and 31-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,826,195 B1 ("Nikolich").

Regarding claim 1,

Nikolich shows in Fig. 8 a plurality of chassis 352, 354, 356, 358, 360, and 362. The cluster shown in Fig. 8 collectively function as a single router (Col. 8, lines 1-2). Nikolich further shows in Fig. 4 a plurality of application modules (claimed processing modules) – CMTS, Ethernet, and SONET (Col. 3, lines 50-54). The application cards

are also called data processing application modules (Col. 6, lines 32-33). Nikolich also shows in Fig. 4, interchassis link port application card and chassis controller/cluster manager. The combination of interchassis link port application card and chassis controller/cluster manager is equivalent to the claimed programmable interconnection.

Nikolich shows in Fig. 11 the application modules 1-11 are connected to application module 12 (claimed interconnection module) via the backplane 420 on the same chassis (Col. 4, line 67- col. 5, line1). Nikolich further shows in Fig. 4 an inter-chassis link port 235 through which the chassis may be linked to another chassis (claimed data connection between the interconnection module on each chassis and the interconnection module on at least one other chassis) (Col. 3, lines 54-55).

Nikolich shows in Fig. 19, a plurality of chassis in a network, wherein when the second chassis is brought up on the network (claimed addition of an additional chassis), link detection protocol (LDP) is used to determine its presence by sending out an LDP message from every link of the current chassis and if the send chassis receives a return signal, the chassis controller identifies the link as the inter-chassis link (ICL), thus making interchassis link port application module 12 a programmable interconnection module as claimed (col. 8, lines 63-67 and col. 9, lines 1-16).

Nikolich further shows in Fig. 11, the application module 12 functions like other application modules 1-11 and every application modules 1-12 has a direct point-to-point link to every other application modules in the chassis via the backplane 420 (claimed connections between individual processing modules on its chassis). However, when the an additional chassis is added to the router, at least one link of the application

module 12 becomes the interchassis link module (claimed changing said switchable connections) connecting at least one application module 1-11 to an interchassis link module of the second chassis (claimed interconnection module on another chassis).

3. Regarding claim 2,

Nikolich shows in Fig. 11 that application modules 422 (processing modules) are connected to chassis controllers 428, 430 (interconnection module) over a chassis management bus 432, which is inherently an electrical connection. Nikolich further shows in Fig. 7 that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (data connections between interconnection modules on different chassis are optical) (Col. 4, lines 33-37).

4. Regarding claim 3,

Nikolich shows in Fig. 4 an interchassis link port application card. In rejection to claim 1, the combination of interchassis link port card and the chassis controller/cluster manager was established as being equivalent to the interconnection module of the applicant. The interchassis link port application card (designated as application 12 in Fig. 11) has plurality of electrical input and output ports 426. Nikolich discloses a Mesh Communication Chip (MCC) that serves as a programmable switching fabric (Col 4. lines 57-65). Nikolich further discloses that the cluster manager keeps a centralized

resource map (connection map) of all the resources, including the location of DSOs available, in the clustered system (Col. 8, lines 52-54).

5. Regarding claim 6,

Nikolich shows in Fig. 11 that each application module 422 (processing module) contains eleven serial links 426 (input and output ports) that run to the backplane (inherently electrical connection) for connecting the application module to every other application module in the chassis. The application module 422 is further connected to chassis controller 428, 430 over a chassis management bus 432 (input and output ports) (Col. 4, lines 63 – col. 5, line 1). The application cards are also called data processing application module (Col. 6, lines 31-33). The backplane is fully meshed meaning that every application module has a direct point-to-point link to every other application module in the chassis through the serial links (processing fabric disposed therebetween) (Col. 5, lines 7-9).

6. Regarding claims 7 and 8,

Nikolich shows in Fig. 11 that each application module 422 (processing module) is connected to chassis controller 428, 430 (interconnection module) over a chassis management bus 432 (inherently through electrical input and output ports) (Col. 4, lines 63 – col. 5, line 1).

7. Regarding claims 10 and 11,

Nikolich shows in Fig. 4 a plurality of application cards (Claim 10 – network interface module; Claim 11- line cards). Fig. 11 further shows various application cards 422 interfacing with an external network through the I/O port, each application card being connected to one or more electrical input and output ports of other application cards (processing modules) through links 426 and the backplane 420.

8. Regarding claim 12,

Nikolich shows in Fig. 11 that application modules 422 (processing modules) are connected to chassis controllers 428, 430 (interconnection module) over a chassis management bus 432, which is inherently an electrical connection. Nikolich further shows in Fig. 7 that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (data connections between interconnection modules on different chassis) (Col. 4, lines 33-37). SONET's fiber optic lines can be OC-48 lines which is 10 gigabits per second (high-bandwidth connections) (Col. 4, lines 28-32). Relatively speaking the electrical connection between the application module and chassis controllers are inherently lower-bandwidth connections.

9. Regarding claim 13,

Nikolich shows in Fig. 11 that packets are switched inside the chassis over the MCC links 426 of the application card 422 (processing module) (Col.5, lines29-30). Fig. 11 shows the electrical input and output ports.

10. Regarding claim 15,

Nikolich discloses that each MCC 424 of Fig. 11 has one link for connecting the module with itself, i.e., a loopback.

11. Regarding claim 16,

Nikolich discloses that the cluster manager (controller) keeps a centralized resource map (connection map) of all the resources (including switch fabric), including the location of DSOs available, in the clustered system (Col. 8, lines 52-54).

12. Regarding claim 17,

Nikolich shows in Fig. 18 a craft interface. The craft interface is a network management interface using 10/100 based Ethernet, which means that it can be remote to the router (Col.7, lines 66-67).

13. Regarding claim 31,

Nikolich shows in Fig. 8 a plurality of chassis 352, 354, 356, 358, 360, and 362 (claimed providing at least one additional chassis). The cluster shown in Fig. 8 collectively function as a single router (Col. 8, lines 1-2). Nikolich further shows in Fig. 4 a plurality of application modules (claimed processing modules) – CMTS, Ethernet, and SONET (Col. 3, lines 50-54). The application cards are also called data processing application module (Col. 6, lines 32-33). Nikolich also shows in Fig. 4, interchassis link port application card and chassis controller/cluster manager. The combination of

interchassis link port application card and chassis controller/cluster manager is equivalent to the programmable interconnection module of the applicant as discussed in the rejection to claim 1. The data connection between each processing module on each additional chassis and the interconnection module on one of the at least one original chassis would operate in the same manner as the direct connection between processing modules of the original chassis and the interconnection module of the additional chassis as discussed above in the rejection to claim 1.

Nikolich further shows in Fig. 4 an inter-chassis link port 235 through which the chassis may be linked to another chassis (claimed data connection between an interconnection module on at least one additional chassis and the at least one interconnection module on one of the at least one original chassis) (Col. 3, lines 54-55).

Nikolich shows in Fig. 11 chassis 200 which has fourteen slots. Twelve of those fourteen slots hold application modules 205, of which may be an interchassis link port 235 through which the chassis can be linked to another chassis (Col. 3, lines 41-43 and 53-55). Nikolich discloses that the chassis controller and cluster manager control the operation and configure each of the modules and can be readily modified and upgraded (Col. 3, lines 34-40), and along with the interchassis link port application module 12, the application module 12 of the original chassis can be reprogrammed to switch connections from between processing modules 1-11 to between a processing module and an interconnection module of the additional chassis as detailed in the rejection to claim 1 (claimed re-programming the at least one interconnection module on each of the at least one original chassis that has a switchable connections such that at least one

processing module on its original chassis is connected to the interconnection module on said at least one additional chassis).

14. Regarding claims 32 and 33,

Nikolich discloses that the chassis controller and cluster manager control the operation and configure each of the modules and can be readily modified and upgraded (Col. 3, lines 34-40). The word "readily" is interpreted to mean that modules can be taken off-line while modifying or programming (Claim 31 – programming the interconnection module of each additional chassis prior to the step of providing the at least one additional chassis; claim 32 - programming the interconnection module of each additional chassis after the step of providing the at least one additional chassis).

15. Regarding claims 34 and 35,

Nikolich shows in Fig. 7 that primary chassis 330 and secondary 332 chassises are linked by a full-duplex link 340 that may be a Fast Ethernet (Claim 34 – electrical connection) or a Packet-over SONET type connection (Claim 35 – optical connection) (Col. 4, lines 34-37).

Establishing a data connection between the interchassis link port application card (claimed interconnection module) on each additional chassis and the interconnection module on one other additional chassis would be the same as establishing a data connection between the interchassis link port application card (claimed interconnection

module) on the original chassis and the interchassis link port application card of the additional chassis as detailed in the rejection to claim 1.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view U.S. Patent No. 6,870,813 B1 ("Raza").

Regarding claims 4 and 5,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich does not disclose that the interconnection module on each chassis includes a signal conditioning module connected to the switch fabric.

Raza discloses that optical network systems consist of equipment, which includes various regeneration and amplification devices (Claim 4 - signal conditioning module; Claim 5 – signal conditioning functionality) (Col 6, lines 51-55).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich to

include/provide a regeneration and amplification device/functionality of Raza to obtain a quality signal that can be effectively switched. One skilled in the art would have been motivated to combine Nikolich with Raza (collectively "Nikolich-Raza") to generate the claimed invention with a reasonable expectation of success.

18. Claims 9, 21-23, 26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of U.S. Patent No. 6,898,205 B1 ("Chaskar").

Regarding claim 9,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 7 of Nikolich that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (inherently optical input and output ports exist since SONET uses fiber optic links) (Col. 4, lines 33-37).

Nikolich does not disclose a plurality of optical-to-electrical and electrical-to-optical conversion units, each respective conversion unit being connected between a respective one of the optical input ports/output ports and a respective subset of the electrical input ports/output ports of the interconnection module.

Chaskar shows in Fig. 1 an optical interface at an optical switching node. Chaskar discloses that a control packet 170 is converted from an optical signal into an electrical signal by an optical-electrical (OE) converter 110 (Col. 3, lines 29-31). The

control packet is converted from electrical domain into an optical domain in an electrical-optical (EO) converter 140 (Col. 3, lines 45-47).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich to include OE and EO converters being respectively connected between a respective one of the optical input ports/output ports and a respective one of the electrical input ports/output ports as disclosed by Chaskar so that signals can be in proper format to be further routed. One skilled in the art would have been motivated to combine Nikolich with Chaskar (collectively "Nikolich-Chaskar") to generate the claimed invention with a reasonable expectation of success.

19. Regarding claim 21,

Nikolich shows in Fig. 4 a plurality of application modules (claimed processing modules) – CMTS, Ethernet, and SONET (Col. 3, lines 50-54).

Nikolich further shows in Fig. 11 that each application module 422 contains eleven serial links 426 (claimed input and output ports) that run to the backplane (claimed electrical connections) for connecting the application module to every other application module in the chassis. The application module 422 is further connected to chassis controller 428, 430 over a chassis management bus 432 (claimed input and output ports) (Col. 4, lines 63 – col. 5, line 1). The application cards are also called data processing application module (Col. 6, lines 31-33). The backplane is fully meshed meaning that every application module has a direct point-to-point link to every other

application module in the chassis through the serial links (claimed processing fabric disposed therebetween) (Col. 5, lines 7-9).

Nikolich also shows in Fig. 4, interchassis link port application card and chassis controller/cluster manager. The combination of interchassis link port application card and chassis controller/cluster manager is equivalent to the programmable interconnection module of the applicant.

Nikolich also shows that the interchassis link port application card (designated as application 12 in Fig. 11) has plurality of electrical input and output ports 426. Nikolich discloses a Mesh Communication Chip (MCC) that serves as a programmable switching fabric (Col 4. lines 57-65) for creating selectively established connections. Nikolich further discloses that the cluster manager keeps a centralized resource map (claimed connection map) of all the resources, including the location of DSOs available, in the clustered system (Col. 8, lines 52-54). Nikolich further discloses that the interchassis link port application card (claimed interconnection module) is operative for changing selectively established connections upon addition of additional chassis as detailed in the rejection to claim 1 concerning the applications modules being connected via the backplane.

Nikolich also shows in Fig. 11 that each application module 422 (claimed processing module) is connected to chassis controller 428, 430 (claimed interconnection module) over a chassis management bus 432 (claimed electrical input and output ports) (Col. 4, lines 63 – col. 5, line 1).

Nikolich shows in Fig. 7 of Nikolich that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (claimed optical input and output ports)(Col. 4, lines 33-37).

Nikolich does not disclose a plurality of optical-to-electrical and electrical-to-optical conversion units, each respective conversion unit being connected between a respective one of the optical input ports/output ports and a respective subset of the electrical input ports/output ports of the interconnection module.

Chaskar shows in Fig. 1 an optical interface at an optical switching node. Chaskar discloses that a control packet 170 is converted from an optical signal into an electrical signal by an optical-electrical (OE) converter 110 (Col. 3, lines 29-31). The control packet is converted from electrical domain into an optical domain in an electrical-optical (EO) converter 140 (Col. 3, lines 45-47).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich to include OE and EO converters being respectively connected between a respective one of the optical input ports/output ports and a respective one of the electrical input ports/output ports as disclosed by Chaskar so that signals can be in proper format to be further routed. One skilled in the art would have been motivated to combine Nikolich with Chaskar (collectively "Nikolich-Chaskar") to generate the claimed invention with a reasonable expectation of success.

20. Regarding claims 22 and 23,

Nikolich-Chaskar shows in Fig. 4 of Nikolich a plurality of application cards (Claim 22 – network interface module; Claim 23- line cards). Fig. 11 further shows various application cards 422 interfacing with an external network through the I/O port, each application card being connected to one or more electrical input and output ports of other application cards (processing modules) through links 426 and the backplane 420.

21. Regarding claim 26,

Nikolich-Chaskar shows in Fig. 11 of Nikolich that packets are switched inside the chassis over the MCC links 426 of the application card 422 (processing module) (Nikolich, col.5, lines29-30). Fig. 11 shows the electrical input and output ports.

22. Regarding claim 28,

Nikolich-Chaskar discloses that each MCC 424 of Fig. 11 of Nikolich has one link for connecting the module with itself, i.e., a loopback.

23. Regarding claim 29,

Nikolich-Chaskar discloses that the cluster manager (controller) keeps a centralized resource map (connection map) of all the resources (including switch fabric), including the location of DSOs available, in the clustered system (Nikolich, col. 8, lines 52-54).

24. Regarding claim 30,

Nikolich-Chaskar shows in Fig. 18 of Nikolich a craft interface. The craft interface is a network management interface using 10/100 based Ethernet, which means that it can be remote to the router (Nikolich, col.7, lines 66-67).

25. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of Chaskar, and further in view of Pub. No. U.S. 2002/0150056 A1 ("Abadi").

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar does not disclose that the programmable switch fabric implements a non-blocking switch

Abadi discloses that crossbar 12 of Fig. 2 is a non-blocking switch.

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the switch fabric of Nikolich-Chaskar to have a non-blocking capability as disclosed by Abadi so that the packets are switched efficiently. One skilled in the art would have been motivated to combine Nikolich-Chaskar with Abadi (collectively "Nikolich-Chaskar-Abadi") to generate the claimed invention with a reasonable expectation of success.

26. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of Chaskar, further in view U.S. Patent No. 6,870,813 B1 ("Raza").

Regarding claims 24 and 25,

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar does not disclose that the interconnection module on each chassis includes a signal conditioning module connected to the switch fabric.

Raza discloses that optical network systems consist of equipment, which includes various regeneration and amplification devices (Claim 24 - signal conditioning module; Claim 25 – signal conditioning functionality) (Col 6, lines 51-55).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich-Chaskar to include/provide a regeneration and amplification device/functionality of Raza to obtain a quality signal that can be effectively switched. One skilled in the art would have been motivated to combine Nikolich-Chaskar with Raza (collectively "Nikolich-Chaskar-Raza") to generate the claimed invention with a reasonable expectation of success.

27. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of Abadi.

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich does not disclose that the programmable switch fabric implements a non-blocking switch

Abadi discloses that crossbar 12 of Fig. 2 is a non-blocking switch.

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the switch fabric of Nikolich to have a non-blocking capability as disclosed by Abadi so that the packets are switched efficiently. One skilled in the art would have been motivated to combine Nikolich with Abadi (collectively "Nikolich-Abadi") to generate the claimed invention with a reasonable expectation of success.

28. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of U.S. Patent 6,058,116 ("Hiscock").

Regarding claim 18,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 4 that each chassis includes a interchassis link port 235 (one port reserved for intra-cluster connection).

Nikolich does not disclose that the chassis are arranged in two or more clusters. Nor does he disclose that the chassis has at least one port reserved for inter-cluster connection.

Hiscock shows in Fig. 7 the concepts of interconnect trunk cluster 110 (two or more clusters). One logical port of each trunk switch 120 is connected to trunk port 137 (one port reserved for inter-cluster connection) (Col. 8, lines 46-49).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the chassis of Nikolich to include having an arrangement of two or more clusters and having one port of a trunk be connected to another port of a trunk in a different cluster as taught by Hiscock so that the clusters can act as a single router. One skilled in the art would have been motivated to combine Nikolich with Hiscock (collectively "Nikolich-Hiscock") to generate the claimed invention with a reasonable expectation of success.

29. Regarding claim 19,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 4 a chassis with an interchassis link port card (chassis interconnection module) that connects to all the chassis in cluster (connections between chassis of a particular one of the clusters are established through the chassis interconnection module).

Nikolich does not expressly disclose that the chassis are arranged in two or more clusters. Nor does disclose that the connection between each pair of clusters are established through the chassis interconnection modules of the clusters of said pair.

Hiscock shows in Fig. 8 two trunk clusters 110 and 210 (two or more clusters).

Fig. 8 further shows that the two clusters are connected by links 125 connecting GEN 2 devices (connection between clusters are through chassis interconnection modules) (Col. 9, lines 6-7).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the chassis of Nikolich to include having an arrangement of two or more clusters and where the clusters are interconnected by a trunk device such as the GEN 2 as taught by Hiscock so that the clusters can act as a single router. One skilled in the art would have been motivated to combine Nikolich with Hiscock (collectively "Nikolich-Hiscock") to generate the claimed invention with a reasonable expectation of success.

30. Regarding claim 20,

Nikolich-Hiscock discloses a system that covers all the limitations of the parent claim.

Nikolich-Hiscock further discloses that the cluster manager keeps a centralized resource map (programmable connections) of all the resources (between different chassis in cluster and between chassis in said cluster and chassis interconnection module of other clusters), including the location of DSOs available, in the clustered system (Nikolich, col. 8, lines 52-54).

RESPONSE TO ARGUMENTS

31. Applicant's arguments filed 1/26/2006 have been fully considered but they are not persuasive.

- In the Remarks beginning on pg. 13 regarding claim 1, the Applicant contends that Nikolich does not teach an interconnection module that is operative to establish switchable connections between individual processing modules on its chassis and between at least one processing module on its chassis and an interconnection module on another chassis. The Applicant further contends that Nikolich does not teach that the interconnection module changes those switchable connections in response to the addition of another chassis.
- The Examiner respectfully disagrees. It is the opinion of the Examiner that the amendment to the independent claim 1 fail to distinguish over Nikolich. As discussed above in the revised rejection to claim 1, Nikolich shows in Fig. 11 that the application modules 1-11 are connected to application module 12 (claimed interconnection module) via the backplane 420 on the same chassis (Col. 4, line 67- col. 5, line1). In other words, before any additional chassis is introduced, the individual application modules, including application module 12 that is connected to the ICL link, is operative to establish connections. Nikolich further shows in Fig. 4 an inter-chassis link port 235 through which the chassis may be linked to another chassis (claimed data connection between the

interconnection module on each chassis and the interconnection module on at least one other chassis) (Col. 3, lines 54-55). Turning now to the limitation requiring the connections between individual processing modules be switched such that at least one processing module and an interconnection module on an additional chassis is connected. Nikolich shows in Fig. 19, a plurality of chassis in a network, wherein when the second chassis is **brought up** (claimed addition of an additional chassis) on the network, link detection protocol (LDP) is used to determine its presence by sending out an LDP message from every link of the current chassis and if the send chassis receives a return signal, the chassis controller identifies the link as the inter-chassis link (ICL). Nikolich discloses that the LDP enables each chassis to identify its ICL links, which must be connected to interconnection module of the additional chassis (col. 8, lines 63-67 and col. 9, lines 1-16). In other words, when the additional chassis is added, the processing modules of the original chassis now have a switchable connection to the interconnection module on the additional chassis.

- In the Remarks beginning on pg. 15 regarding claim 31, the Applicant contends that Nikolich does not disclose that the interchassis links can be "re-programmed" such that a processing module on the original chassis

can be connected to an interconnection module on at least one additional chassis.

- The Examiner respectfully disagrees. It is the opinion of the Examiner that the amendment to the independent claim 31 fail to distinguish over Nikolich. As discussed above concerning claim 1, link detection protocol (LDP) determine the presence of additional chassis when it is brought up by sending out an LDP message from every link of the current chassis and if the send chassis receives a return signal, the chassis controller identifies the link as the inter-chassis link (ICL). Nikolich further discloses that the LDP enables each chassis to identify its ICL links, which must be connected to interconnection module of the additional chassis (col. 8, lines 63-67 and col. 9, lines 1-16). This procedure is interpreted by the Examiner as the "re-programming" of interconnection module of the original chassis such that the processing module on the original chassis is connected to the interconnection module on the additional chassis.

- In the Remarks beginning on pg. 19, regarding claim 21, the Applicant contends that Nikolich does not teach an interconnection module that is operative for creating selectively established connections, and then changing those connections upon the addition of an additional chassis.
- The Examiner respectfully disagrees. It is the opinion of the Examiner that the amendment to the independent claim 21 fail to distinguish over

Nikolich. As discussed above concerning claim 1, the application modules 1-11 are connected to application module 12 (claimed interconnection module) via the backplane 420 on the same chassis (claimed selectively established connections)(Col. 4, line 67- col. 5, line1). As discussed above concerning claims 1 and 31, the LDP is used by the chassis controller to identify the ICL of the chassis to change the selectively established connections upon the addition of another chassis.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US20060007946A1 (Kastenholz) teaches interconnect network for operation within a communication node.
- US6522646B1 (Madonna) teaches expandable telecommunications system.

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Sol whose telephone number is (571) 272-5949. The examiner can normally be reached on M-F 7:30am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

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5/3/2006